

J1033 U.S. PTO
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05/08/01

LIST OF REFERENCES CITED BY APPLICANT (use as many sheets as necessary)				Application Number: Not yet assigned Filing Date: Herewith First Named Inventor: Hung-Hsiang Jonathan CHAO Group Art Unit: Not yet assigned Examiner Name: Not yet assigned
Sheet	1	of	1	Attorney Docket No.: Poly-17/APP

OTHER REFERENCES - NON-PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume, issue number(s), publisher, country, where published, source		
RLM	AA.	N. W. McKeown, "Scheduling Algorithms for Input-Queued Cell Switches", PhD Thesis, University of California at Berkeley, (1995).		
RLM	AB.	C. Y. Lee and A. Y. Oruc, "A Fast Parallel Algorithm for Routing Unicast Assignments in Benes Networks", <u>IEEE Trans. on Parallel and Distributed Sys.</u> , Vol. 6, No. 3, pp. 329-333 (March 1995).		
RLM	AC.	T. T. Lee and S-Y Liew, "Parallel Routing Algorithms in Benes-Clos Networks", <u>Proc. IEEE INFOCOM '96</u> , pp. 279-286 (1996).		
RLM	AD.	N. McKeown, M. Izzard, A. Mekkittikul, W. Ellersick and M. Horowitz, "Tiny-Tera: A Packet Switch Core", <u>IEEE Micro.</u> , pp. 26-33 (Jan-Feb. 1997).		
RLM	AE.	T. Chaney, J. A. Fingerhut, M. Flucke, J. S. Turner, "Design of a Gigabit ATM Switch", <u>Proc. IEEE INFOCOM '97</u> , PP. 2-11 (April 1997).		
RLM	AF.	F. M. Chiussi, J. G. Kneuer, and V. P. Kumar, "Low-Cost Scalable Switching Solutions for Broadband Networking: The ATLANTA Architecture and Chipset", <u>IEEE Commun. Mag.</u> , pp. 44-53 (Dec. 1997).		
RLM	AG.	J. Turner and N. Yamanaka, "Architectural Choices in Large Scale ATM Switches", <u>IEICE Trans. Commun.</u> , Vol. E81-B, No. 2, pp. 120-137 (Feb. 1998).		
RLM	AH.	H. J. Chao and J-S Park, "Centralized Contention Resolution Schemes for a Large-Capacity Optical ATM Switch", <u>Proc. IEEE ATM Workshop '97</u> , (Fairfax, VA, May 1998).		
RLM	AI.	N. McKeown, "The iSLIP Scheduling Algorithm for Input-Queued Switches", <u>IEEE/ACM Transactions on Networking</u> , Vol. 7, No. 2, (April 1999).		
RLM	AJ.	N. McKeown, A. Mekkittikul, V. Anantharam, and J. Walrand, "Achieving 100% Throughput in an Input-Queued Switch", <u>IEEE Trans. on Communications</u> , Vol. 47, No. 8, pp. 1260-1267 (Aug. 1999).		
RLM	AK.	E. Oki, N. Yamanaka, Y. Ohtomo, K. Okazaki and R. Kawano, "A 10-Gb/s (1.25 Gb/s x 8) 4 x 2 0.25- μ m CMOS/SIMOX ATM Switch Based on Scalable Distributed Arbitration", <u>IEEE J. of Solid-State Circuits</u> , Vol. 34, No. 12, pp. 1921-1934 (Dec. 1999).		
RLM	AL.	J. Chao, "Saturn: A Terabit Packet Switch Using Dual Round-Robin", <u>IEEE Communications Magazine</u> , pp. 78-84, (Dec. 2000).		

Examiner Signature	<i>Shenda S. Murphy</i>	Date Considered	11-10-04
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Unique citation designation number. 2 Applicant is to place a check mark here if English language translation is attached.